

What Is Claimed Is:

1 1. A charged-device model (CDM) electrostatic discharge (ESD)
2 protection circuit for an integrated circuit (IC), the ESD
3 protection circuit comprising:

4 an ESD clamp device, coupled to a pad and a substrate having
5 a first conductivity type, the ESD clamp device being closed
6 under normal power operation; and

7 a functional component, formed on the substrate and coupled
8 to the pad, the functional component having a first well of the
9 first conductivity type and an isolating region of a second
10 conductivity type, the second conductivity type being the
11 reversed polarity of the first conductivity type, and the
12 isolating region isolating the first well from the substrate;
13 the functional component transmitting signals between the IC and
14 an external linkage under normal power operation.

1 2. The CDM ESD protection circuit in claim 1, wherein when the
2 isolating region comprises a second well surrounding the first
3 well and a deep well under the first well.

1 3. The CDM ESD protection circuit in claim 1, wherein the
2 isolating region is coupled to a first power supply and the first
3 well is coupled to a second power supply.

1 4. The CDM ESD protection circuit in claim 1, wherein the
2 functional component comprises a metal-oxide semiconductor
3 (MOS) having the second conductivity type in the first well.

1 5. The CDM ESD protection circuit in claim 1, wherein the ESD
2 clamp device comprises an MOS diode having two ends respectively
3 coupled to the pad and the substrate.

1 6. The CDM ESD protection circuit in claim 1, wherein the ESD
2 clamp device is a two-stage ESD protection circuit, having a
3 primary ESD protection circuit coupled between the pad and the
4 substrate, a secondary ESD protection circuit coupled between
5 the functional component and the substrate, and a resistor
6 coupled between the functional component and the pad.

1 7. The CDM ESD protection circuit in claim 1, wherein the first
2 conductivity type is an N type, and the second conductivity type
3 is p type.

1 8. The CDM ESD protection circuit in claim 1, wherein the first
2 conductivity type is a p type, and the second conductivity type
3 is N type.

1 9. A charged-device model (CDM) electrostatic discharge (ESD)
2 protection circuit for an input port of an integrated circuit
3 (IC), the ESD protection circuit comprising:

4 an ESD clamp device, coupled to a pad and a substrate having
5 a first conductivity type, under normal power operation, the ESD
6 clamp device being closed; and

7 an MOS component having a second conductivity type, formed
8 in a first well on the substrate and coupled to the pad; an
9 isolating region having the second conductivity type being
10 formed between the first well and the substrate to separate the
11 first well and the substrate, the second conductivity type being

12, the reversed polarity of the first conductive type, and under
13 normal power operation, the MOS component transmitting signals
14 from the pad into the IC.

1 10. The CDM ESD protection circuit in claim 9, wherein a gate
2 of the MOS component is coupled to the pad.

1 11. The CDM ESD protection circuit in claim 9, wherein the
2 source of the MOS component is coupled to an internal power line.

1 12. The CDM ESD protection circuit in claim 11, wherein the CDM
2 ESD protection circuit further comprises an ESD protection
3 circuit coupled between the gate of the MOS component and the
4 internal power line.

1 13. The CDM ESD protection circuit in claim 12, wherein the ESD
2 protection circuit at the input port is an gate-grounded MOS
3 component.

1 14. The CDM ESD protection circuit in claim 11, wherein the
2 first well is coupled to the internal power line.

1 15. A charged-device model (CDM) electrostatic discharge (ESD)
2 protection circuit for an output port of an integrated circuit
3 (IC), the ESD protection circuit comprising:

4 an ESD clamp device, coupled to a pad and a substrate having
5 the first conductivity type, under normal power operation, the
6 ESD clamp device being closed; and

7 an MOS component having a second conductivity type, formed
8 in a first well on the substrate and coupled to the pad; an

9 isolating region having the second conductivity type being
10 formed between the first well and the substrate to separate the
11 first well and the substrate, the second conductivity type being
12 the reversed polarity of the first conductive type, and under
13 normal power operation, the MOS component transmitting signals
14 from the IC to the pad.

1 16. The CDM ESD protection circuit in claim 15, wherein a drain
2 of the MOS component is coupled to the pad, a source of the MOS
3 component and the first well are coupled to an I/O power line.

1 17. The CDM ESD protection circuit in claim 15, wherein a
2 plurality of diodes are disposed between the I/O power line and
3 an internal power line.

1 18. A CDM ESD protection circuit, suitable for an I/O port of
2 a high voltage IC, the CDM ESD protection circuit comprises:
3 an ESD clamp device, coupled between a pad and a p-type
4 substrate, the ESD clamp device being closed under normal power
5 operation; and

6 a first NMOS (N-type metal-on-semiconductor) component
7 formed on a P-type first isolated well on the substrate, an
8 N-type isolating region being formed to separate the P-type
9 first isolated well and the substrate; the NMOS component having
10 a gate coupled to a high power line, a first source/drain coupled
11 the pad, and a second source/drain coupled to an input buffer;
12 and

13 an output driver comprising a second and a third NMOS
14 component respectively formed in a P-type second isolated well
15 on the substrate and connected in series; an N-type second

16 isolating region formed between the P-type second isolated well
17 and the substrate, a gate of the second NMOS component, coupled
18 to the high Power line, a drain of the second NMOS component
19 coupled to the pad, a source of the second NMOS component coupled
20 to a drain of the third NMOS component, a source of the third
21 NMOS component coupled to an I/O low power line, and a gate of
22 the third NMOS component being to a pre-output driver.

1 19. The CDM ESD protection circuit in claim 18, wherein the
2 first isolated well is coupled to an internal low power line,
3 the second isolated well is coupled to the I/O low power line.

1 20. The CDM ESD protection circuit in claim 19, wherein a
2 plurality of diodes are disposed between the internal low power
3 line and the I/O low power line.

1 21. The CDM ESD protection circuit in claim 18, wherein the ESD
2 clamp device comprises a forth NMOS component and a fifth NMOS
3 component, connected in series between the pad and I/O low power
4 line, a gate of the forth NMOS component is coupled to the high
5 power line, and a gate of the fifth NMOS component is coupled
6 to the I/O low power line.

22. The CDM ESD protection circuit in claim 18, wherein an ESD
protection resistor is formed between the first NMOS component
and the pad.